PATENT ABSTRACTS OF JAPAN

(11)Publication number:

07-161703

(43) Date of publication of application: 23.06.1995

(51)Int.CI.

H01L 21/31 C23C 16/50 C23F 4/00

H01L 21/768

(21)Application number : 05-339565

(71)Applicant : RICOH CO LTD

(22)Date of filing: 03.12.1993

}

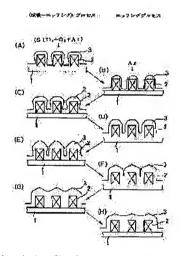
(72)Inventor: FUSE AKIHIRO

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To restrain damage on a semiconductor device by a bias ECR plasma CVD method, and form a high reliability insulating film with excellent controllability which has an excellent step-covering form.

CONSTITUTION: Firstly a bias ECR plasma CVD process is performed for a specified period by introducing film forming material gas and argon gas, and a silicon oxide film 3 having an overhang form to some extent is formed on a metal wiring 2 as shown by (A). Secondly the introduction of film forming gas is interrupted, and a sputter etching process is performed for a specified period. By primarily etching the overhang part of the silicon oxide film 3, a form shown by (B) is obtained. After that, the bias ECR plasma CVD process



and the sputter etching are sequentially repeated, and an insulating film 3 having excellent step-covering form wherein the part between the metal wirings 2 and 2 is filled without voids and flattened as shown by (H) is finally formed.

LEGAL STATUS

[Date of request for examination]

27.06.2000

Searching PAJ

[Date of sending the examiner's decision of 16.04.2002 rejection] [Kind of final disposal of application other than the examiner's decision of rejection or application converted registration] [Date of final disposal for application] [Patent number] [Date of registration] [Number of appeal against examiner's decision of rejection] [Date of requesting appeal against examiner's decision of rejection] [Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office